A SYSTEM AND METHOD FOR DETECTING DESIGN ERRORS IN INTEGRATED CIRCUITS

ABSTRACT OF THE INVENTION

The present invention is embodied in a system and method for detecting design errors, such as errors in an integrated circuit design. The present invention uses a probabilistic model, such as a Bayesian Belief Network (BBN), to detect design errors at any point in the design process by using information about the current design in combination with historical design error data from previous designs. Detection of design errors in evolving or completed designs is accomplished by monitoring conditions, or patterns of conditions produced by design tasks that have historically been associated with symptoms related to design errors in previous designs. The probabilistic model of the present invention is used in conjunction with fuzzy inferencing to identify and rank condition sets of the present design against historical conditions and condition sets from prior designs. Consequently, where an exact match between present and historical conditions or condition sets is not identified, the inexact pattern matching afforded by inferential analysis of the conditional probabilities generated by the probabilistic model of the present invention is utilized to identify the probability that the same or similar design error exists in the present design as was identified in the prior design. In addition, the present invention identifies potential candidate errors and conditions for further investigation based on proximity and similarity of preceding and succeeding tasks, conditions, and design attributes. The results of the probabilistic detection of design errors are preferably presented to the user both textually and graphically in an interactive computer program environment.